IN THE CLAIMS

Claims 1-30 (Canceled)

31. (New) A semiconductor device comprising:

a plurality of inner leads extending around a semiconductor chip;

a thin sheet-shaped insulating member supporting said semiconductor chip and joined to an end portion of said respective inner leads;

a conductive wire for connecting surface electrodes of said semiconductor chip and said inner leads corresponding thereto;

a seal portion in which said semiconductor chip, said wire, and said insulating member are resin-sealed; and

a plurality of outer leads linked to said inner leads and exposed from said seal portion,

wherein a length of a shorter side of a main surface of said semiconductor chip formed in a quadrilateral shape is less than or equal to twice a distance from a tip of the inner leads arranged at the farthest location from a center line of the semiconductor chip in a plane direction, to said semiconductor chip.

32. (New) A semiconductor device comprising:

a plurality of inner leads extending around a semiconductor chip;

a thin sheet-shaped insulating member supporting said semiconductor chip and joined to an end portion of said respective inner leads;

a conductive wire for connecting surface electrodes of said semiconductor chip and said inner leads corresponding thereto;

a seal portion in which said semiconductor chip, said wire, and said insulating member are resin-sealed; and

a plurality of outer leads linked to said inner leads and exposed from said seal portion,

wherein an arrangement pitch of said surface electrodes of said semiconductor chip is 1/2 as much as or less than a minimum value of a tip pitch between said inner leads adjacent to each other.

33. (New) A semiconductor device comprising:

an insulating member having an upper surface and a lower surface;

a semiconductor integrated chip having a plurality of bonding pads; and

first, second, third, and fourth conductive leads disposed respectively in the left, right, upper, and lower sides of said semiconductor integrated chip with respect to a plane direction of said semiconductor integrated chip,

wherein each of said first to fourth conductive leads includes a first end having a lower surface connected to a front surface of said insulating member and an upper surface capable of being wire-connected to one of said bonding pads,

wherein said first ends of said first and second conductive leads are respectively disposed along a phantom line, which extends across said semiconductor integrated chip from the left side of said semiconductor integrated chip to the right side thereof, and

wherein a length of said phantom line passing across said semiconductor integrated chip is dimensionally equal to or less than a total of the distance between said semiconductor integrated chip and said first conductive lead and that between said semiconductor integrated chip said second conductive lead, and further said semiconductor device includes a resin covering said first ends, said semiconductor

integrated chip, and said insulating member and exposing other ends opposite to said first ends.

34. (New) The semiconductor device according to claim 31, wherein said insulating member is a tape substrate.

35. (New) The semiconductor device according to claim 31, wherein said insulating member is a glass-containing epoxy substrate.

36. (New) The semiconductor device according to claim 31, wherein said semiconductor chip is mounted on a surface of an inner lead arrangement side of said insulating member.

37. (New) The semiconductor device according to claim 31, wherein said inner leads and said insulating member are joined by an adhesive layer, and said semiconductor chip is thicker than a total of said insulating member and said adhesive layer in thickness.

38. (New) The semiconductor device according to claim 31, wherein said insulating member and said inner leads are joined by adhesive layers of a pressure sensitive adhesive

double coated tape having a tape base, on both front and rear surfaces whose said adhesive layers are disposed.

39. (New) The semiconductor device according to claim 31, wherein said inner leads and said insulating member are joined by an adhesive layer, and said adhesive layer is provided to connect the portion between said inner leads in an inner lead arrangement side of said insulating member.

40. (New) The semiconductor device according to claim 31, wherein said inner leads and said insulating member are joined by an adhesive layer, and said adhesive layer is provided throughout the entirety of a surface of an inner lead arrangement side of said insulating member.

41. (New) The semiconductor device according to claim 31, wherein said inner leads and said insulating member are joined by an adhesive layer, and said adhesive layer is disposed just on an inner lead joining portion of said insulating member.

42. (New) The semiconductor device according to claim 35, wherein said glass-containing epoxy substrate contains alumina particles.

43. (New) A semiconductor device comprising:

a semiconductor chip having a plurality of surface electrodes;

a conductive wire connected between a thin-plate-shaped substrate supporting said semiconductor chip and said surface electrodes of said semiconductor chip;

a resin-sealing portion having upper and lower surfaces and four side surfaces linked therebetween, and sealing said semiconductor chip, said wire, and said thin-plate-shaped substrate; and

a plurality of leads each having a first portion connected to said surface electrodes of said semiconductor chip and said wire, and a second portion exposed from said resin-sealing portion,

wherein each end of said plurality of leads and said thin-plate-shaped substrate are connected, and

wherein said second portions of said plurality of leads are respectively exposed along four sides of said lower surface of said resin-sealing portion.